77. ML Global Ltd.
78. Newfast Co., Ltd.
79. Noah Enterprise Co., Ltd.
80. Nytaps Taiwan Corporation
81. Pao Shen Enterprises Co., Ltd.
82. Par Excellence Industrial Co., Ltd.
83. Pengteh Industrial Co., Ltd.
84. Pneumax Corp.
85. Printech T Electronics Corporation
86. Pro-an International Co., Ltd.
87. Pronto Great China Corp.
88. Professional Fasteners Development Co., Ltd.
89. P.S.M. Fasteners (Asia) Limited
90. Qi Ding Enterprise Co., Ltd.
91. Right Source Co., Ltd.
92. Rodex Fasteners Corp.
93. Rong Chang Metal Co., Ltd.
94. San Shing Fastech Corporation
95. SBSCQ Taiwan Limited
96. Shanxi Pioneer Hardware Industrial Co., Ltd.
97. Somax Enterprise Co., Ltd.
98. Spec Products Corporation
99. Star World Product and Trading Co., Ltd.
100. Sumeeko Industries Co., Ltd.
101. Sunshine Spring Co., Ltd.
102. Suntec Industries Co., Ltd.
103. Supreme Fasteners Corp.
104. Szu I Industries Co., Ltd.
105. Tag Fasteners Sdn. Bhd.
106. Taifas Corporation
107. Taiwan Geer-Tai Works Co., Ltd.
108. Taiwan Quality Fastener Co., Ltd.
109. Team Builder Enterprise Limited
110. Techno Associates Taiwan Co., Ltd.
111. Techup Development Co., Ltd.
112. TG Co., Ltd.
113. Tianjin Jinchi Metal Products Co. Ltd.
114. Topps Wang International Ltd.
115. Ume-Pride International Inc.
116. Unistrong Industrial Co., Ltd.
117. United Nail Products Co. Ltd.
118. Vanguard International Co., Ltd.
119. Wa Tai Industrial Co., Ltd.
120. Win Fastener Corporation
121. WTA International Co., Ltd.
122. Wumax Industry Co., Ltd.
123. Wyser International Corporation
124. Yeun Chang Hardware Tool Company Limited
125. Yng Tran Enterprise Company Limited
126. Yoh Chang Enterprise Company Limited
127. Yow Chern Company
128. Yumark Enterprises Corporation
129. Yu Tai World Co., Ltd.
130. Zenith Good Enterprise Corporation

[FR Doc. 2024–02003 Filed 1–31–24; 8:45 am]

BILLING CODE 3510–DS–P

DEPARTMENT OF COMMERCE

National Institute of Standards and Technology

Notice of Availability of Draft Programmatic Environmental Assessment for Modernization and Internal Expansion of Existing Semiconductor Fabrication Facilities Under the CHIPS Incentives Program

AGENCY: National Institute of Standards and Technology, Department of Commerce.

ACTION: Notice; availability of a Draft Programmatic Environmental Assessment; extension of comment period.

SUMMARY: The National Institute of Standards and Technology (NIST) is extending the period for submitting comments on the Draft Programmatic Environmental Assessment (PEA) for the modernization and internal expansion of existing semiconductor fabrication facilities under the CHIPS Incentives Program. The original deadline for public comments was January 25, 2024. NIST is extending the deadline until February 9, 2024.

DATES: The comment period for the notice published December 27, 2023, at 88 FR 89372, is extended. Comments must be received on or before February 9, 2024. Comments received after January 25, 2024, and before publication of this notice are deemed to be timely. Those who have already submitted comments need not resubmit.

ADDRESSES: The PEA is available for download and review at *https://www.nist.gov/chips/national-environmental-policy-act-nepa,* under the heading ''NEPA Public Involvement.''

You may submit comments on the PEA by the following methods:

Electronic Submission: Submit all electronic public comments via email to *ChipsNEPA@chips.gov* citing ''Modernization PEA'' in the subject line. NIST will accept comments in attached Word or PDF formats or within the body of the email.

By mail: Comments can also be mailed to the CHIPS Incentives Program at: Department of Commerce; HCHB Room 7419; ATTN: CPO Environmental Division; 1401 Constitution Ave NW, Washington, DC 20230.

Instructions: Comments sent by any other method, to any other address or individual, or received after the end of the comment period, may not be considered by NIST. All comments received are a part of the public record; commenters should not include personal identifying information (*e.g.,* name, address, etc.), confidential business information, or otherwise sensitive information. NIST will accept anonymous comments. The most helpful comments include a specific recommendation, explain the reason for any recommended change, and provide supporting information. NIST will consider all relevant comments received on or before the closing date.

FOR FURTHER INFORMATION CONTACT: David Frenkel, NIST, telephone number 240–204–1960, email *David.Frenkel@chips.gov.*

SUPPLEMENTARY INFORMATION: In a **Federal Register** notice dated December 27, 2023 (88 FR 89372), NIST announced the availability of the Draft PEA for the modernization and internal expansion of existing semiconductor fabrication facilities under the CHIPS Incentives Program. NIST has prepared the draft PEA in accordance with the National Environmental Policy Act (NEPA, 42 U.S.C. 4321 *et seq.*) and the Council on Environmental Quality's (CEQ) NEPA implementing regulations (40 CFR parts 1500 through 1508). The PEA addresses financial assistance for the modernization or internal expansion of existing current-generation and mature-node commercial facilities within their existing footprint throughout the U.S.

The original deadline for public comments was January 25, 2024. NIST has received a request for an extension of the comment period due to the length and technical content of the document. NIST is therefore extending the deadline until February 9, 2024.

Authority: This notice is provided pursuant to NEPA and CEQ's NEPA implementing regulations (40 CFR 1506.6).

Tamiko Ford,

NIST Executive Secretariat.

[FR Doc. 2024–02042 Filed 1–31–24; 8:45 am]

BILLING CODE 3510–13–P

DEPARTMENT OF COMMERCE

National Institute of Standards and Technology

CHIPS Manufacturing USA Institute

AGENCY: National Institute of Standards and Technology, Department of Commerce.

ACTION: Notice of Intent (NOI).

SUMMARY: The CHIPS Research and Development Office (CHIPS R&D) intends to announce an open competition for a new Manufacturing

USA Institute. The expected competition will seek to establish one (1) Manufacturing USA Institute focused on the topic of digital twins for semiconductor manufacturing, packaging, and assembly and the validation of such digital twins in a physical prototyping facility. This NOI is provided to allow potential applicants sufficient time to develop meaningful collaborations among industry, academic, Federal laboratory, and state/local government partners.

FOR FURTHER INFORMATION CONTACT: All inquiries may be directed to Mahesh Mani (301–975–2000) via email to *research@chips.gov,* with a subject line stating: 'MFG USA CHIPS Institute Competition.' All answers, which will be provided at the sole discretion of CHIPS R&D, will be posted on the NIST competition website at *https://www.nist.gov/chips/chips-RD-funding-opportunities.*

SUPPLEMENTARY INFORMATION:

Purpose. The CHIPS Research and Development Office (CHIPS R&D) intends to announce an open competition for a new Manufacturing USA Institute, pursuant to 15 U.S.C. 4656(f). The expected competition will seek to establish one (1) Manufacturing USA Institute focused on the topic of digital twins for semiconductor manufacturing, packaging, and assembly and the validation of such digital twins in a physical prototyping facility. This CHIPS Manufacturing USA Institute will be established and operate in accordance with 15 U.S.C. 278s, as amended. For general planning purposes, the minimum expected NIST commitment will be approximately $200 million over a 5-year period. CHIPS R&D expects to leverage private sector and other non-Federal investments on a substantially greater than 1:1 basis.

This NOI is provided to allow potential applicants sufficient time to develop meaningful collaborations among industry, academic, Federal laboratory, and state/local government partners. Details in this NOI should also inform discussions at a planned February 2024 CHIPS Manufacturing USA Institute Industry Day where the government will solicit feedback on the NIST plans and timelines for the Institute. CHIPS R&D expects to announce the competition via a Notice of Funding Opportunity (NOFO) on *Grants.gov* at *https://www.grants.gov* in the second quarter of calendar year 2024. CHIPS R&D reserves the right to refine program structure, cost, co-investment requirements, and other program details in the eventual NOFO. In the event of inconsistencies between the NOI and the NOFO, the NOFO shall take precedence.

Background

Program Background: The CHIPS and Science Act appropriated approximately $50 billion to the Department of Commerce—$39 billion in incentives to onshore semiconductor manufacturing and $11 billion to advance U.S. leadership in semiconductor R&D. Congress authorized NIST to establish not more than three Manufacturing USA Institutes focused on semiconductor manufacturing. Manufacturing USA Institutes are public-private partnerships that bring together industry of all sizes, universities and community colleges, federal agencies, and state organizations to accelerate innovation by investing in industrially relevant technologies that advance specific technology sectors. Institutes may address the full spectrum of advanced manufacturing challenges, such as innovation for manufacturing processes, novel materials, cross cutting enabling technology, supply chain integration methodology and education and workforce development.

After receiving extensive public input, CHIPS R&D determined that a single institute with both regionally-focused programs and meaningful cross-region participation will best meet the CHIPS R&D program goals of strengthening U.S. technology leadership, accelerating ideas to market, and realizing a robust semiconductor workforce. Despite substantial existing investment in proprietary digital twin technology, the United States lacks a comprehensive environment for collaborative development and validation of semiconductor industry digital twins. In establishing a single institute with national reach, CHIPS R&D seeks to enable the seamless integration of digital twin models into U.S. semiconductor manufacturing, advanced packaging, and assembly, enabling rapid adoption of innovations and enhancing domestic competitiveness for decades. The CHIPS Manufacturing USA Institute will foster a collaborative environment to significantly expand innovation, bring tangible benefits to manufacturers of all sizes, strengthen diverse research institutions, and ensure a national reach in workforce development.

CHIPS Manufacturing USA Institute Objectives: CHIPS R&D expects that the NOFO soliciting proposals will seek to achieve the following objectives:

1. Significantly reduce U.S. chip development and manufacturing costs, such as by improving capacity planning, optimizing production, and enabling real-time process adjustments.

2. Improve development cycle time and accelerate adoption of innovative semiconductor manufacturing technologies, including breakthrough tools, manufacturing equipment, materials, and manufacturing processes validated at the shared facility.

3. Advance digital twin-enabled curricula and best practices for training the semiconductor workforce nationwide.

4. Create a digital twin marketplace for industry, including entrepreneurs, to access digital models and manufacturing process flows and to de-risk digital twin development and implementation.

CHIPS R&D expects to solicit proposals demonstrating strong industry leadership capable of catalyzing collaboration in software development relevant to digital twins (including but not limited to electronic design automation tools), semiconductor manufacturing, advanced packaging, and assembly. Expected activities include establishing a shared physical facility where companies can experiment while protecting proprietary information; enabling industry-relevant research projects; leveraging a shared marketplace that enables data aggregation across companies, while protecting proprietary data, to make powerful digital twins available at low cost; and operating an education and workforce development program, which may include partnerships with educational institutions.

Competition Information: Once the open competition has been announced, further information may be found at *https://www.nist.gov/chips/chips-RD-funding-opportunities.*

System for Award Management: In anticipation of the NOFO, CHIPS R&D encourages potential applicants to complete the following steps, which are required to submit applications for Federal assistance:

- Register with the System for Award Management (SAM) at *https://www.sam.gov.* CHIPS R&D strongly encourages applicants to register for SAM.gov as early as possible. While this process ordinarily takes between three days and two weeks, in some circumstances it can take six or more months to complete due to information verification requirements. Recipients will be required to maintain an active registration in SAM and re-validate registration annually.
- Register for a *Grants.gov* (*https://www.grants.gov/*) account. It is advisable also to go to ''manage subscriptions'' on *Grants.gov* and sign

up to receive automatic updates when amendments to a funding opportunity are posted.

Disclaimer. This NOI does not constitute a solicitation. No applications may be submitted in response to this NOI. Any inconsistency between information within this NOI and the eventual NOFO announcing the CHIPS Manufacturing USA Institute award competition shall be resolved in favor of the NOFO.

Authority: DOC CHIPS activities were authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116–283, often referred to as the CHIPS Act).

Tamiko Ford,

NIST Executive Secretariat.

[FR Doc. 2024–02025 Filed 1–31–24; 8:45 am]

BILLING CODE 3510–13–P

DEPARTMENT OF COMMERCE

National Institute of Standards and Technology

CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Materials and Substrates Research and Development

AGENCY: National Institute of Standards and Technology, Department of Commerce.

ACTION: Notice of Intent (NOI).

SUMMARY: The CHIPS Research and Development Office (CHIPS R&D) intends to announce, via a Notice of Funding Opportunity (NOFO), an open competition for new research and development (R&D) activities to establish and accelerate domestic capacity for advanced packaging substrates and substrate materials, a key technology for manufacturing semiconductors. CHIPS R&D anticipates making available up to approximately $300,000,000 for multiple awards in amounts up to approximately $100,000,000 per award, not including voluntary co-investment, over up to 5 years and made through cooperative agreements or other transactions. The purpose of this NOI is to offer preliminary information to potential applicants, facilitating the development of meaningful partnerships and strong, responsive proposals.

FOR FURTHER INFORMATION CONTACT: All inquiries may be directed to Chris Greer (301–975–2000) via email to *research@chips.gov,* with a subject line stating: '2024–NIST–CHIPS–NAPMP–01 Questions.' All answers, which will be provided at the sole discretion of CHIPS R&D, will be posted on the NIST competition website at *https://www.nist.gov/chips/chips-RD-funding-opportunities.*

SUPPLEMENTARY INFORMATION:

Purpose. The CHIPS Research and Development Office (CHIPS R&D) intends to announce, via a Notice of Funding Opportunity (NOFO), an open competition for new research and development (R&D) activities to establish and accelerate domestic capacity for advanced packaging substrates and substrate materials, a key technology for manufacturing semiconductors. CHIPS R&D anticipates making available up to approximately $300,000,000 for multiple awards in amounts up to approximately $100,000,000 per award, not including voluntary co-investment, over up to 5 years and made through cooperative agreements or other transactions. Co-investment (cost share) is not required in this program. CHIPS R&D will, however, give preference to applications that demonstrate committed co-investment in their application.

The purpose of this NOI is to offer preliminary information to potential applicants, facilitating the development of meaningful partnerships and strong, responsive proposals. CHIPS R&D intends to announce the competition no later than March 2024 by posting the NOFO on *Grants.gov* at *https://www.grants.gov.* More information about the expected CHIPS R&D NAPMP Materials and Substrates competition will then be available at the CHIPS for America website at *https://www.nist.gov/chips/chips-RD-funding-opportunities.*

Background. Emerging technologies like artificial intelligence, advanced telecommunications, biomedical devices, and autonomous vehicles require leap-ahead advances in microelectronics capabilities. Improving all aspects of system performance to support the breadth of new semiconductor applications will require advanced packaging and related capabilities, such as heterogeneous integration, to address the need to integrate multi-component-assemblies with large numbers of interconnects to achieve a degree of integration that blurs the line between chip and package.

In particular, the ability to ''scale-down and scale-out'' will be critical, where ''scale-down'' refers to shrinking the size of the features on the package and ''scale-out'' refers to increasing the number of chips assembled on the substrate.

Materials and substrates are foundational to achieving the necessary advancements. Moreover, materials and substrates R&D, particularly applied R&D, is critical to expanding the U.S. packaging ecosystem.

CHIPS R&D Mission and Goals: The CHIPS and Science Act appropriated approximately $50 billion to the Department of Commerce—$39 billion in incentives to onshore semiconductor manufacturing and $11 billion to advance U.S. leadership in semiconductor R&D. Within CHIPS for America, the mission of CHIPS R&D is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities. NAPMP, one of multiple CHIPS R&D initiatives, seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States.

Within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, profitable, onshore packaging industry where advanced node chips manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities. In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities produce the diverse and capable workforce needed for the success of the domestic packaging sector.

Materials and Substrates NOFO Objectives: Three major R&D areas have the potential to make a significant impact on domestic advanced packaging capabilities: organic materials and substrates (including fan-out); glass materials and substrates; and semiconductor-based substrates. Within these areas, CHIPS R&D intends to fund R&D activities that establish and promote relevant domestic capability and capacity, with the following objectives:

1. Accelerate domestic R&D and innovation in advanced packaging materials and substrates;

2. Transition domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;