clearance was subsequently sought and approved by OMB on October 30, 2020 (OMB No. 0607–1013; Exp. 10/30/2023).

Affected Public: Households.

Frequency: Households will be selected once to participate in a 20-minute survey.

Respondent's Obligation: Voluntary.

Legal Authority: Title 13, United States Code, Sections 8(b), 182 and 193.

This information collection request may be viewed at *www.reginfo.gov.* Follow the instructions to view the Department of Commerce collections currently under review by OMB.

Written comments and recommendations for the proposed information collection should be submitted within 30 days of the publication of this notice on the following website *www.reginfo.gov/public/do/PRAMain.* Find this particular information collection by selecting ''Currently under 30-day Review—Open for Public Comments'' or by using the search function and entering either the title of the collection or the OMB Control Number 0607–1013.

Sheleen Dumas,

Department PRA Clearance Officer, Office of the Chief Information Officer, Commerce Department.

[FR Doc. 2022–01237 Filed 1–21–22; 8:45 am]

BILLING CODE 3510–07–P

DEPARTMENT OF COMMERCE

[Docket Number: 220119–0024]

Incentives, Infrastructure, and Research and Development Needs To Support a Strong Domestic Semiconductor Industry

AGENCY: Department of Commerce.

ACTION: Notice; request for information.

SUMMARY: The Department of Commerce (Department), with the assistance of the National Institute of Standards and Technology (NIST), is seeking information in order to inform the planning and design of potential programs to: Incentivize investment in semiconductor manufacturing facilities and associated ecosystems; provide for shared infrastructure to accelerate semiconductor research, development, and prototyping; and support research related to advanced packaging and advanced metrology to ensure a robust domestic semiconductor industry. Responses to this Request for Information (RFI) will inform the planning of the Department of Commerce for the potential implementation of these programs.

DATES: Comments must be received by 5:00 p.m. Eastern time on March 25, 2022. Written comments in response to this RFI should be submitted in accordance with the instructions in the **ADDRESSES** and **SUPPLEMENTARY INFORMATION** sections below. Submissions received after that date may not be considered.

ADDRESSES:

For Comments

To respond to this RFI, please submit electronic public comments via the Federal e-Rulemaking Portal.

1. Go to *www.regulations.gov* and enter DOC–2021–0010 in the search field,

2. Click the ''Comment Now!'' icon, complete the required fields, and

3. Enter or attach your comments.

Comments sent by any other method, to any other address or individual, or received after the end of the comment period, may not be considered.

Comments containing references, studies, research, and other empirical data that are not widely published should include electronic copies of the referenced materials. Please do not submit additional materials.

All relevant comments received in response to the RFI will be made publicly available on *www.regulations.gov.* All submissions, including attachments and other supporting materials, will become part of the public record and subject to public disclosure. Personal information, such as account numbers or Social Security numbers, or names of other individuals, should not be included. Submissions will not be edited to remove any identifying or contact information. Do not submit confidential business information, or otherwise sensitive or protected information. Comments that contain profanity, vulgarity, threats, or other inappropriate language or content will not be considered.

For Public Meetings/Webcast

The Department may hold future workshops to explore in more detail questions raised in the RFI. Notice and details about any potential future workshop dates and registration deadlines, etc. will be announced at *www.nist.gov/semiconductors.*

FOR FURTHER INFORMATION CONTACT:

For questions about this Notice, contact: George Orji, in the NIST Program Coordination Office, at *george.orji@nist.gov,* (301) 975–3475.

Please direct media inquiries to Jennifer Huergo in the NIST Public Affairs Office at *jennifer.huergo@nist.gov,* (301) 975–6343.

SUPPLEMENTARY INFORMATION:

Background

Semiconductors are fundamental to nearly all modern industrial and national security activities, and they are essential building blocks of critical and emerging technologies, such as artificial intelligence, autonomous systems, next generation communications, and quantum computing.

The U.S. semiconductor industry has historically dominated many parts of the semiconductor supply chain, such as research and development (R&D), chip design, and manufacturing. Over the past several years, the U.S. position in the global semiconductor industry has faced numerous challenges. In 2019, the United States accounted for 11 percent of global semiconductor fabrication capacity, down from 13 percent in 2015 and continuing a long-term decline from around 40 percent in 1990. Much of the overseas semiconductor manufacturing capacity is in Taiwan (led by Taiwan Semiconductor Manufacturing Company), South Korea (led by Samsung), and, increasingly, China.[1]

Furthermore, the fragility of the current global semiconductor supply chain was put squarely on display in 2020. The industry faced significant disruptions as a result of the coronavirus pandemic, a fire affecting a major supplier in Japan, and a severe winter storm that disabled production in facilities in Texas for several days.[2] Together these events and other factors such as pandemic-induced shifts in consumer demand contributed to a global semiconductor shortage that affected multiple manufacturing sectors which rely on semiconductors as critical components for their finished products. Especially severely hit was the automotive industry, which saw plants idled for months.[3]

To strengthen the U.S. position in semiconductor R&D and manufacturing, Congress authorized a set of programs in Title XCIX (''Creating Helpful Incentives to Produce Semiconductors in America'') of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (Pub. L. 116–283). This comprehensive set of programs is intended to restore U.S. leadership in semiconductor manufacturing by providing incentives and encouraging investment to expand manufacturing

[1] *https://www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf.*

[2] *https://www.ept.ca/features/global-chip-shortage-a-timeline-of-unfortunate-events/.*

[3] *https://hbr.org/2021/02/why-were-in-the-midst-of-a-global-semiconductor-shortage.*

capacity for the most advanced semiconductor designs as well as those of more mature designs that are still in high demand, and would grow the research and innovation ecosystem for microelectronics and semiconductor R&D in the U.S., including the investments in the infrastructure necessary to better integrate advances in research into semiconductor manufacturing.

President Biden's American Jobs Plan [4] calls for at least $50 billion to fund this set of programs, and Congress is considering legislation with similar funding levels over the next 5 years.[5] If funded as proposed in the United States Innovation and Competitiveness Act (USICA) S.1260:

- $39B would be directed to incentivize the construction or modernization of facilities in the U.S. for semiconductor fabrication, assembly, testing, advanced packaging, or R&D; and
- Another $11.2B would support several R&D and infrastructure investments including the establishment of a National Semiconductor Technology Center (NSTC), investments in advanced packaging, the creation of a Manufacturing USA institute targeting semiconductors, and expansion of NIST's metrology R&D in support of semiconductor and microelectronics R&D.

Goals of This Request for Information

This RFI invites the public to inform the design and implementation of the set of potential Department of Commerce programs laid out in the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116–283) (NDAA). Comments are invited from all interested parties, domestic or foreign, including semiconductor manufacturers; industries associated with or that support the semiconductor industry, such as materials providers, equipment suppliers, manufacturers, and designers; trade associations, educational institutions, and government entities; original equipment manufacturers; semiconductor buyers; semiconductor industry investors; and any other stakeholders.

The Department of Commerce seeks input on the potential set of programs in general and the following topics specifically:

- Semiconductor Financial Assistance Program—The incentive program, under Section 9902 of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116–283) (NDAA), should it be funded by Congress, will be competitively awarded to private entities, consortia of private entities, or public-private consortia to incentivize the establishment, expansion, or modernization of semiconductor manufacturing facilities and supporting infrastructure. Funds will target production of leading-edge and mature logic chips, analog chips essential to critical industries and defense needs, and memory chips.
- National Semiconductor Technology Center—Under Section 9906 (c) of the NDAA, the National Semiconductor Technology Center (NSTC) is authorized to conduct advanced semiconductor manufacturing R&D and prototyping; establish an investment fund; and promote and expand workforce training and development opportunities. As authorized, the Department currently envisions the NSTC as a hub of talent, knowledge, investment, equipment and toolsets that tackles Moore's Law transitions, research into new materials, architectures, processes, devices, and applications, and, most importantly, bridges the gap between R&D and commercialization. Should NSTC be funded by Congress, companies would be expected to co-invest and participate in developing their own intellectual property together with NSTC staff, and to collaborate with other companies, universities and Federal labs on pre-competitive technologies and designs.
- Advanced Packaging Manufacturing Program—Advanced packaging and heterogeneous integration present a significant opportunity for innovation, leading to better yields, lower costs, greater functionality, reuse of intellectual property blocks enabling accelerated design iterations and customization, and improved energy efficiency. With support, there is a unique opportunity for U.S.-based equipment suppliers and manufacturers to lead in this critical area.
- Workforce Development Needs of the Industry—The growth and sustainment of the Nation's semiconductor industry depends on a highly skilled workforce capable of meeting current and future needs of the public and private sectors.

The goal of this RFI is to gather input that will be utilized to develop resources and programs to protect and extend U.S. semiconductor technology leadership; secure the supply of chips for critical, commercial and non-commercial U.S. sectors; and promote the economic viability of U.S. industry in R&D, manufacturing, and other critical areas of the semiconductor value chain, should the Creating Helpful Incentives for the Production of Semiconductors (CHIPS) for America Act programs be funded by Congress.

Public Meeting

The Department may hold future workshops to explore in more detail questions raised in the RFI. Notice and details about any potential future workshop dates and registration deadlines will be announced at *www.nist.gov/semiconductors.*

Details About Responses to This Request for Information

When addressing the topics below, commenters may address the practices of their organization or a group of organizations with which they are familiar. If desired, commenters may provide information about the type, size, and location of the organization(s). Provision of such information is optional and will not affect the Department's full consideration of the comment.

All relevant comments received in response to the RFI will be made publicly available on *www.regulations.gov.* Comments containing references, studies, research, and other empirical data that are not widely published should include electronic copies of the referenced materials. All submissions, including attachments and other supporting materials, will become part of the public record and will be subject to public disclosure. Personal information, such as account numbers or Social Security numbers, or names of other individuals, should not be included. Do not submit confidential business information, or otherwise sensitive or protected information. Comments that contain profanity, vulgarity, threats, or other inappropriate language or content will not be considered.

Specific Requests for Information

The following statements and questions cover the major topic areas about which the Department seeks comment. They are not intended to limit the topics that may be addressed. Responses may include any topic believed to inform U.S. Government efforts in developing recommendations for supporting the growth and sustainment of a robust domestic semiconductor manufacturing sector to meet the current and future needs of the public and private sectors, regardless of whether the topic is included in this document.

[4] *https://www.whitehouse.gov/briefing-room/statements-releases/2021/03/31/fact-sheet-the-american-jobs-plan/.*

[5] S. 1260 Section 1002 (A) 2 (i) through (v).

Respondents are encouraged to respond to any or all of the following questions and topic areas, and may address related topics. Please identify the questions or topic areas each of your comments addresses. Responses may include estimates. Please indicate where the response is an estimate. Respondents may organize their submissions in response to this RFI in any manner.

All relevant responses that comply with the requirements listed in the **DATES** and **ADDRESSES** sections of this RFI will be considered.

The Department is requesting information related to the following topics:

Semiconductor Financial Assistance Program

1. The term ''semiconductor'' is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of ''semiconductor'' for purposes of a semiconductor manufacturing incentives program?

2. Section 9902 permits a ''consortium'' of public and private entities to apply for funding. What factors would public and private entities consider determining whether to apply for funding as part of consortium? How would private entities determine whether to work with a public entity as part of a consortium? How would a private entity consider working with other private entities (such as customers, equipment manufacturers, or capital providers) as part of a consortium?

3. Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?

4. Based on the criteria outlined in Section 9902 of the NDAA, what do you see as presenting the biggest challenges for an organization to develop an application for funding as part of a consortium, and how long do you estimate it would take for an organization to prepare the required materials?

5. Subject to the criteria and eligibility requirements outlined in Section 9902 of the NDAA, what other factors should the Secretary consider as important when reviewing applications for Federal financial assistance?

6. Section 9902 defines a covered entity to include, among other things public-private consortia, which could include partnerships between semiconductor firms and customers, suppliers, investors, state and local governments, federally funded research and development centers (FFRDCs), and other entities. How can Section 9902 incentives be designed and deployed to encourage additional and new private capital investment in the semiconductor ecosystem? What can be learned from other technology infrastructure development programs that use such partnerships (*e.g.,* data center facilities or communications infrastructure) that may be applicable to semiconductor facilities?

7. How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?

8. How can Federal funds incentivize the creation of a broad semiconductor ecosystem that includes producers of semiconductor manufacturing equipment and other upstream suppliers? What are the largest supply imbalances with respect to manufacturing equipment, tools, materials, and chemicals that need to be addressed by U.S. investment?

9. How can the program ensure that semiconductor startups and small and midsized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, including intellectual property products such as ''Process Design Kits''?

10. Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?

11. Section 9902 requires a covered entity to make commitments to invest in workers and communities, including through training and education benefits and programs to expand employment opportunity for economically disadvantaged individuals. What constitutes a baseline commitment to worker training in the semiconductor industry and what other workforce investments should be considered? Are there international best practices or cooperation upon which your company finds beneficial? What other community investments should be considered beyond worker training and employment opportunities? How can worker training, other workforce commitments, and other community commitments be maximized and how should program participants be held accountable to their commitments? What types of programs exist, or could be expanded, to improve access for economically disadvantaged individuals to these workforce and community commitments and opportunities?

12. Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?

13. What is the industry's environmental footprint in terms of its land and resource use, air quality and water quality impact, hazardous or other special-handling material needs, and greenhouse gas emissions impact? What is the industry currently planning or implementing on these dimensions and how will the environmental footprint likely change over the next decade as a result? What effect will semiconductor chip customers' ''net zero'' announcements or other related incentives have on the industry's environmental footprint? What opportunities exist for the industry to move to a smaller and more sustainable footprint, and how can such opportunities be used to create a stronger domestic market for chips produced with a smaller footprint?

National Semiconductor Technology Center

1. Based on the functions outlined in section 9906(c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap

between R&D and commercialization. What attributes are most important for the NSTC to possess or provide to the community (*e.g.,* ease of access, a broad suite of leading edge tools managed as central facility, a collaborative research environment)? What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?

2. As authorized, the NSTC would have to be able to work with a wide range of research groups from industry, academia, and government, some of whom will be contributing valuable intellectual property. What approaches to intellectual property should be in place to protect the foundational contributions of members while enabling maximum collaboration and innovation amongst the research community supported by NSTC? What IP issues create unique challenges for middle- and late-stage prototyping collaborations versus early-stage research, design and proof-of-concept collaborations?

3. The federal government has several programs that support microelectronics and associated R&D across many agencies, federal labs, university labs, corporate labs, and other for-profit and nonprofit entities. What existing domestic R&D activities, assets, intellectual property, knowledge and expertise should be incorporated or otherwise connected to the NSTC, and are any international in nature? How should the NSTC interface with federal labs, university labs, corporate labs and other existing institutions of R&D and prototyping to ensure that R&D projects are supported throughout the technology maturation process so that public research funds are able to improve R&D productivity and attract additional private and venture investment?

4. How should the NSTC connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

5. How should the NSTC ensure that it can identify and invest in what comes next after the first wave of needs are identified in the initial years? To what extent does the semiconductor ecosystem need a long-term roadmap of application requirements, technical needs, and gaps in materials, tooling and equipment, and process capabilities in order to guide future R&D investments? How can the NSTC's investments best support an open roadmap of this type, and how should the NSTC interface with other governments or allied international R&D programs, such as those established under Section 9905 of the FY2021 NDAA, to enable such a roadmap? What existing technology forums, roadmaps, or other initiatives should be incorporated into such efforts?

6. The NSTC is envisioned as a public-private partnership. What are the most suitable models of public-private partnership for the R&D and prototyping gaps that the NSTC is envisioned to address? What are the roles of the public participants and the private-sector participants in this partnership, including any international participants? How should governance structures, program objectives, investment criteria, and oversight and accountability requirements be structured to maximize the transformative potential of the NSTC in the US R&D ecosystem?

7. What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities? How can the NSTC ensure that smaller and medium-sized companies and startups have access to facilities, expertise, and intellectual property that public funds support?

8. For those who currently participate or have participated in a ''research consortium'' (either domestic or international) made up of public and private partners, what are the important lessons learned or best practices that the NSTC should follow?

9. What attributes or capabilities of the NSTC would make it attractive and beneficial for companies, universities, and other agencies to want to send employees for assignments at the NSTC? What types of research and training opportunities should be made available at the NSTC for students and early career staff?

10. For organizations that currently utilize an external semiconductor ''fab'' as part of their R&D efforts, what services or processes are currently missing in the U.S. ecosystem that the NSTC should provide? Are there specific toolsets that the NSTC should own and operate or provide access to?

11. As authorized, the NSTC could establish an investment fund, in partnership with the private sector, to support startups and collaborations between startups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, including advanced metrology and characterization for leading-edge manufacturing processes, and for security and supply chain verification. How should this investment fund be structured, and what should be the roles of the public and private sectors in capitalizing, operating, and overseeing the fund and selecting its investment targets? Should the investment fund focus on early-stage investing, late-stage investing, or other stages of the process? How should the fund interact with existing private capital, both venture capital and established investment capital, and how can the fund sustain itself through its investments?

12. How should the NSTC's investments and focus overlap or complement the investments and capabilities of foreign institutions such as the Interuniversity Microelectronics Center (imec) in Belgium or the French Laboratoire d'électronique des technologies de l'information (CEA-Leti)?

Advanced Packaging Manufacturing Program

1. Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- Analog device packaging
- Automotive
- Defense and aerospace
- Energy generation, transmission, conversion, and storage
- Harsh environments
- High performance computing, quantum computing, data centers
- Integrated photonics
- Integrated power electronics
- Internet of Things
- Mature packaging
- Medical, health & wearables
- MEMS and sensor electronics
- Mobile telecommunications
- Other?

2. Please describe the R&D core-competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- Alternative materials to mitigate impact of supply chain disruptions
- Artificial intelligence for design of packaging
- Assembly and test

- Emerging materials
- Heterogeneous integration, chip stacking, and related technologies.
- High-density substrates
- Metrology
- Modeling and simulation
- Package-level design/codesign tools for electrical, thermal and mechanical design of complex packages
- Printed circuit boards
- Safety and security
- Software, firmware, new concepts in programming
- Standards
- Test solutions to assure yield in complex packages
- Thermal solutions
- Tooling
- Other?

3. A proposed National Advanced Packaging Manufacturing Program could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, work force development, and supply chain development. Please describe the most critical needs on which the program should focus.

4. What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver? Examples include but are not limited to:

- ''Leading edge'' tools
- Characterization services
- Collaboration across multiple universities and multiple companies
- Development of education and workforce development infrastructure, including building a pipeline of skilled workers
- Easy to access facility, with different processes and tools
- Expert resident staff for custom development
- International participation
- Intellectual property protection for inventors
- Open access to intellectual property
- Post fabrication infrastructure
- Other?

5. What factors are critical to enable a National Advanced Packaging Manufacturing Program to provide a successful packaging R&D hub(s)?

6. Identify processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for facilities provided by a National Advanced Packaging Manufacturing Program. How might organizations access such facilities?

7. How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?

8. How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

9. Describe anticipated needs in education and workforce development, including retraining and upskilling, in the semiconductor packaging area. How adequate is it currently, and what are future expectations of need? How should the workforce training pipeline be developed?

Semiconductor Workforce

1. What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

2. What strategies have been most effective in addressing the shortages? Which states or countries have created the most effective strategies for different types of workforce needs to build, equip, and run semiconductor manufacturing and R&D facilities?

What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions? To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners to establish training and/or skill certification programs? To what extent do employers in the semiconductor sector partner with other employers to create joint training programs?

3. What types of apprenticeship programs or existing partnerships involving workforce development issues in the semiconductor sector should the Department be aware of? What role can unionized labor play in worker training and workforce development, including for economically disadvantaged individuals?

4. What have been successful mechanisms used by employers in the semiconductor sector to work with local high schools, career and technical education programs, community colleges, or universities to recruit and train workers?

5. Are there any current or planned initiatives in the semiconductor sector to strengthen and expand the recruitment of women and underrepresented minorities, including promotion of such careers at K–12 levels?

6. To what extent, and for what occupations, do organizations in the semiconductor sector use the H1–B Program to fill positions?

7. Are there opportunities to design the semiconductor incentive program to ensure that worker skills shortages do not hinder companies from expanding operations?

Sreenivas Ramaswamy,

Senior Policy Advisor, Office of Policy and Strategic Planning, U.S. Department of Commerce.

[FR Doc. 2022–01305 Filed 1–21–22; 8:45 am]

BILLING CODE 3510–20–P

DEPARTMENT OF COMMERCE

National Institute of Standards and Technology (NIST)

Information Collection Activities; Submission to the Office of Management and Budget (OMB) for Review and Approval; Comment Request; Baldrige Executive Fellows Program

The Department of Commerce will submit the following information collection request to the Office of Management and Budget (OMB) for review and clearance in accordance with the Paperwork Reduction Act of 1995, on or after the date of publication of this notice. We invite the general public and other Federal agencies to comment on proposed, and continuing information collections, which helps us assess the impact of our information collection requirements and minimize the public's reporting burden. Public comments were previously requested via the **Federal Register** on November 16, 2021, during a 60-day comment period. This notice allows for an additional 30 days for public comments.

Agency: National Institute of Standards and Technology (NIST), Commerce.

Title: Baldrige Executive Fellows Program.

OMB Control Number: 0693–0076.

Form Number(s): None.

Type of Request: Regular, extension of current information collection.

Number of Respondents: 24 per year.

Average Hours per Response: 1 hour to gather materials.